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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
WANG, JIN CHENG

ART UNIT	PAPER NUMBER
2672	6

DATE MAILED: 08/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/724,197	GETTEMY ET AL.	
	Examiner	Art Unit	
	Jin-Cheng Wang	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Amendment

1. The amendment filed on 6/24/2003 has been entered. Claims 1, 10, and 18 have been amended.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim), Hannah U.S. Patent No. 5,038,297 (hereinafter Hannah) and Yuri et al. U.S. Patent No. 5,805,149 (hereinafter Yuri).

4. Claim 1:

(1) Matsuzaki teaches a display unit (e.g., figures 1-2) comprising:

a display panel comprising a pixel matrix comprising: an (m * n) pixel display memory window region; and an x pixel border region for only displaying a display attribute (e.g., figures 6-7B), wherein said border region surrounds said display memory window region (e.g., figures 6-7B; column 5, lines 25-60);

a memory for containing image data for generating an image within said display memory window region (figures 6-7B; column 5, lines 25-60);

a display controller (e.g., the display control circuit, SVGA 21 of figure 3) coupled to said memory (e.g., VRAM 22), coupled to receive said display attribute from said border attribute register (e.g., the border producing circuit or registers of figures 1-3; column 5, lines 5-60; column 7, lines 10-65), and coupled to control said display panel (figures 1-7B; column 5, lines 5-60), said display controller for generating a first set of signals (i.e., pixel data) for rendering said image within said display memory window region and for generating a second set of signals (i.e., border pixel data) for display said display attribute within said border region (e.g., column 3, lines 6-25; column 7, lines 5-67; column 8, lines 1-35; column 13, lines 48-60).

(2) However, it is not clear whether Matsuzaki implicitly teaches a frame buffer for storing the pixel data for the display memory window region.

(3) Kim/Hannah/Yuri teaches implicitly a frame buffer for storing the pixel data for the display memory window region (See Kim column 8, lines 55-67; Hannah 2, lines 1-20; Yuri column 4, lines 45-67).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the Kim or Hannah or Yuri's frame buffer into Matsuzaki's display unit because Matsuzaki suggests a graphics control circuit fetching pixel data from VRAM 22 (Matsuzaki figures 1-3; column 6, lines 3-65) while Kim/Hannah/Yuri teaches a VRAM corresponds to a frame buffer memory (region) and therefore the claimed limitation suggests an obvious modification of Matsuzaki.

(5) One having the ordinary skill in the art would have been motivated to do this because Hannah teaches that the frame buffer is typically a collection of video random access memory

(VRAM) while Kim teaches that the video frame buffer memory is constructed from VRAM (See Kim column 8, lines 55-67; Hannah 2, lines 1-20) and Yuri teaches a VRAM is a frame memory for storing image data in combination with the controller (Yuri column 4, lines 45-67).

5. Claim 2-4, 7-8 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim), Hannah U.S. Patent No. 5,038,297 (hereinafter Hannah) and Yuri et al. U.S. Patent No. 5,805,149 (hereinafter Yuri), further in view of Ogawa et al. U.S. Patent No. 6,018,331 (hereinafter Ogawa) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla).

6. Claim 2-4, 7, 8:

(1) The claim 2-4, 7,8 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of (1) the second set of signals being generated within invalid timing windows with respect to the frame buffer region; (2) a first portion of the second set of signals being generated x clock cycles before valid data for the frame buffer region commences and a second portion of the second set of signals being generated in an invalid horizontal timing window that ends x clock cycles after valid data for the frame buffer region; (3) a third portion of the second set of signals being generated in an invalid vertical timing window that commences x horizontal pulses before a first valid horizontal line commences of a frame and a forth portion of the second set of signals being generated in an invalid vertical timing window that ends x horizontal pulses after the end of the last valid horizontal line of the frame; (4) x being equal 2; (5) the frame buffer region comprising 160 rows and 160 columns of pixels.

As shown in the rejection of claim 1, Matsuzaki/Kim/Hannah teaches the claimed invention of a display unit.

(2) However, it is not clear whether Matsuzaki/Kim/Hannah implicitly teaches the additional claimed limitation as recited in claims 2-4.

(3) Singla, Ogawa and Yuri teaches the additional claimed limitation as recited in claims 2-4. Namely, Singla, Ogawa and Yuri teach the claimed limitation of (1) the second set of signals being generated within invalid timing windows with respect to the frame buffer region (Singla figures 2-5; Ogawa column 5, lines 4-67; column 6, lines 1-67; Ogawa figures 7-9; Yuri figure 7); (2) a first portion of the second set of signals being generated x clock cycles before valid data for the frame buffer region commences and a second portion of the second set of signals being generated in an invalid horizontal timing window that ends x clock cycles after valid data for the frame buffer region (Singla figures 2-5; Ogawa column 5, lines 4-67; column 6, lines 1-67; Ogawa figures 7-9; Yuri figure 7); (3) a third portion of the second set of signals being generated in an invalid vertical timing window that commences x horizontal pulses before a first valid horizontal line commences of a frame and a forth portion of the second set of signals being generated in an invalid vertical timing window that ends x horizontal pulses after the end of the last valid horizontal line of the frame (Singla figures 2-5; Ogawa column 5, lines 4-67; column 6, lines 1-67; Ogawa figures 7-9); 4) x being equal 2 (Ogawa figure 7; Singla figure 2; Yuri figure 7); (5) the frame buffer region comprising 160 rows and 160 columns of pixels (Ogawa figure 7; Singla figure 2; Yuri figure 7).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated Singla, Ogawa and Yuri's timing generator into Matsuzaki/Kim/Hannah/Yuri's display device

because Matsuzaki suggests partial rewrite driving using display start line address, the number of continuous display lines, the total number of lines, the total number of pixels, and the border region to the line address producing circuit, thereby obtaining partial display information (Matsuzaki column 8, lines 1-67). Matsuzaki discloses a plurality of display formats for the effective display region (Matsuzaki column 8, lines 1-67). Therefore the claimed limitation suggests an obvious modification of Matsuzaki/Kim/Hannah/Yuri.

(5) One having the ordinary skill in the art would have been motivated to do this because Ogawa teaches timing chart for the horizontal/vertical timing intervals to generate the timing signals so that the input image signal is displayed in the center and its periphery is made a frame, the drive of picture elements corresponding to the frame can be carried out during the horizontal/vertical blanking intervals (Ogawa column 5, lines 4-67; column 6, lines 1-67; Yuri figure 7).

7. Claim 5, 6, 9 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim) and Hannah U.S. Patent No. 5,038,297 (hereinafter Hannah) and Yuri et al. U.S. Patent No. 5,805,149 (hereinafter Yuri).

Claim 5:

The claim 5 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the display attribute of the border region comprising a color attribute and an intensity attribute. However, Matsuzaki further discloses the claimed limitation of the display

attribute of the border region comprising a color attribute and an intensity attribute (e.g., Matsuzaki figures 6-8).

Claim 6:

The claim 6 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the display panel being a thin film transistor liquid crystal display panel. However, Matsuzaki further discloses the claimed limitation of the display panel being a thin film transistor liquid crystal display panel (e.g., Matsuzaki column 1, lines 20-60; column 5, lines 1-25).

Claim 9:

The claim 9 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of background display attribute register. Matsuzaki further discloses the claimed limitation of background display attribute register (e.g., Matsuzaki figures 6-8).

8. Claims 10-17 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of in view of Kim et al. U.S. Patent No. 5,355,443 (hereafter Kim) and Hannah U.S. Patent No. 5,038,297 (Hannah), further in view of Ogawa et al. U.S. Patent No. 6,018,331 (hereafter Ogawa) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla).

9. Claim 10:

The claim 10 encompasses the same scope of invention as that of claims 1 and 2. The claim 10 is rejected for the same reasons set forth in claims 1 and 2.

Claims 11-12:

The claim 11, or 12 encompasses the same scope of invention as that of claims 1-4. The claim 11 is rejected for the same reasons set forth in claims 1-4.

Claim 13:

The claim 13 encompasses the same scope of invention as that of claims 1-5. The claim 13 is rejected for the same reasons set forth in claims 1-5.

Claim 14:

The claim 14 encompasses the same scope of invention as that of claims 1-6. The claim 14 is rejected for the same reasons set forth in claims 1-6.

Claim 15:

The claim 15 encompasses the same scope of invention as that of claims 1-7. The claim 15 is rejected for the same reasons set forth in claims 1-7.

Claim 16:

The claim 16 encompasses the same scope of invention as that of claims 1-8. The claim 16 is rejected for the same reasons set forth in claims 1-8.

Claim 17:

The claim 17 encompasses the same scope of invention as that of claims 1-9. The claim 16 is rejected for the same reasons set forth in claims 1-9.

10. Claims 18-23 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim) and Hannah U.S. Patent No. 5,038,297 (hereinafter Hannah) and Yuri et al. U.S. Patent No. 5,805,149 (hereinafter Yuri), further in view of Ogawa et al. U.S. Patent No. 6,018,331 (hereafter Ogawa) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla) and He et al. U.S. Patent No. 6,323,849 (He).

Claims 18-23:

The claim 18-23 encompasses the same scope of invention as that of claims 1-9 except additional claimed limitation of a portable electronic device. However, He/Yuri further discloses the additional claimed limitation of a portable electronic device (He column 1, lines 20-35; Yuki column 14, lines 1-15).

Remarks

11. Applicant's arguments, filed 06/24/2003, paper number 5, have been fully considered but they are not deemed to be persuasive.

12. Applicant argues in essence with respect to claim 1 and similar claims that:

> "...the present invention, as presently claimed in currently amended Independent Claims 1, 10, and 18 specifically recites a display panel comprising a pixel border region for only displaying a display attribute, wherein the pixel border region is distinct from the frame buffer region that displays images. As such, the pixel border region does not display images, and only displays a display attribute. Moreover, that display attribute is

applied across all the pixels of the border region. Thus, Applicants respectfully submit that the currently amended independent Claims 1, 10, and 18 of the present invention are neither anticipated nor rendered obvious by the Sawada et al. reference, and are in condition for allowance."

This is not found persuasive because

Matsuzaki teaches a display unit (e.g., figures 1-2) comprising:

a display panel comprising a pixel matrix comprising: an (m * n) pixel display memory window region; and an x pixel border region for only displaying a display attribute (e.g., figures 6-7B), wherein said border region surrounds said display memory window region (e.g., figures 6-7B; column 5, lines 25-60);

a memory for containing image data for generating an image within said display memory window region (figures 6-7B; column 5, lines 25-60);

a display controller (e.g., the display control circuit, SVGA 21 of figure 3) coupled to said memory (e.g., VRAM 22), coupled to receive said display attribute from said border attribute register (e.g., the border producing circuit or registers of figures 1-3; column 5, lines 5-60; column 7, lines 10-65), and coupled to control said display panel (figures 1-7B; column 5, lines 5-60), said display controller for generating a first set of signals (i.e., pixel data) for rendering said image within said display memory window region and for generating a second set of signals (i.e., border pixel data) for display said display attribute within said border region (e.g., column 3, lines 6-25; column 7, lines 5-67; column 8, lines 1-35; column 13, lines 48-60).

Therefore, Matsuzaki/Kim/Hannah/Yuri fulfills the amended claim 1 as currently drafted.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (703) 605-1213. The examiner can normally be reached on 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (703) 305-4713. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-6606 for regular communications and (703) 308-6606 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 395-3900.

jcw
August 18, 2003

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600